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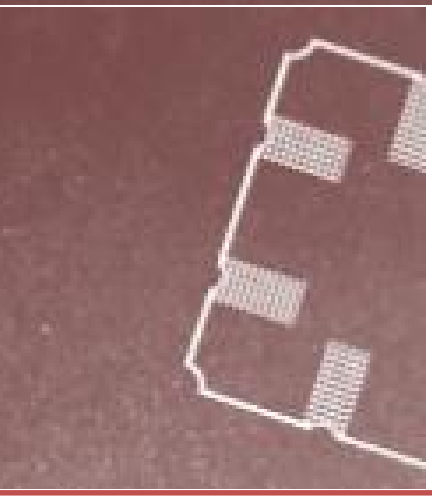

Introduction to Low Jitter LVDS and PECL Clock Oscillator Designs :

Over the last fifteen years improvements in data communications transport technology has made it possible to transmit data and voice at ever increasing levels of megabits per second. As these speeds increase, the transmission of this data from one point to another becomes the limiting factor for the overall system performance. In these circumstances low-voltage differential signaling (LVDS) is gaining increased market share across the data communications landscape.

LVDS is a high speed digital interface that has become the solution in applications where low power and high noise immunity (minimal jitter influence) is required to achieve the smallest bit error rates during broadband transmission. LVDS uses differential signals with low voltage swings (means lower power dissipation) to transmit data at high rates. Differential signals are contrasted from traditional single-ended signals such as CMOS in that two complementary signal lines are used to transmit data instead of one line referenced to ground.

While PECL logic signals enjoy many of the same noise immunity properties as LVDS due to being a differential signal format, the larger voltage swings required of PECL circuits consume significantly more power at the same frequencies of operation than does LVDS. Thus, the industry continues to see a steady replacement of PECL solutions with LVDS where applicable and cost effective for clock oscillator requirements. As a result Dynamic Engineers offers both output types to satisfy all possible legacy and new design opportunities.

XO3001 Clock Oscillator with Low Jitter LVDS or PECL Outputs :

The XO3001 clock oscillator family offers a 5x7 mm surface mount ceramic carrier package with a choice between differential outputs using LVDS or PECL logic. Overall frequency stability of +/- 30 ppm can be offered which includes : drift over -40C to 85C ; make-tolerance at room temperature ; long term aging ; frequency change with power supply and load variation ; reflow frequency shift ; and changes due to shock and vibration.

Frequency range of operation is from 19.44 MHz to 320 MHz.

The customer can select either a 2.5 or 3.3 supply voltage option. Maximum current drain will be 100 mA maximum when PECL logic is implemented depending upon operating frequency. Maximum current using LVDS outputs will be between 50 and 65 mA depending upon operating frequency.

Integrated phase jitter in a 12KHz to 20MHz bandwidth will range from 0.3 ps to 0.7 ps maximum.

Our four most popular qualified XO3001 differential output devices have operating frequencies of 25, 100, 125, and 156.25 MHz. Key performance parameters are presented on the next four pages for each part number variation.

XO7500-G2 Clock Oscillator with Low Jitter LVDS Outputs :

The XO7500-G2 represents a new generation of integrated circuit technology which is able to deliver 27 mA maximum current drain using either a 2.5V or 3.3V supply with LVDS differential outputs. This represents a 50% reduction in operating power over more mature technologies.

Operating frequencies from 40 MHz to 200 MHz have been optimized to achieve typical phase jitter of 0.3 ps in a 12KHz to 20MHz bandwidth.

Frequency stability over -40C to 85C can be +/- 25 ppm or +/- 50 ppm depending upon application requirement.